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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,091	08/28/2001	Tae-sung Jung	5649-886	5816

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EXAMINER
CAO, CHUN

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,091	JUNG ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,34,35,37,43 and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34,35 and 37* is/are allowed.

6)☒ Claim(s) *1-25,27-29,43 and 44* is/are rejected.

7)☒ Claim(s) *26 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30, 34, 35, 37, 43 and 44 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The drawings were received on 5/3/05. These drawings are accepted.

4. Claims 5, 6, 8-13, 19 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitations" the predetermined delay time" in lines 3-6. There are insufficient antecedent basis for this limitation in the claim.

Claim 6 is rejected because they incorporate the deficiencies of claim 5.

Claim 8 recites the limitations" the specification of the memory module" in line 5, "the predetermined delay information" in line 7, "the received delay control information" in line 8. There are insufficient antecedent basis for this limitations in the claim.

Claims 9-13 are rejected because they incorporate the deficiencies of claim 8.

Claim 19 recites the limitations" the predetermined delay time" in lines 3-6. There are insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitations" the predetermined delay time" in lines 3-6. There are insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7-10, 12-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClannahan (McClannahan), U.S. patent no. 6,438,670 in view of Ryan (Ryan), U.S. patent no. 6,418,495.

As per claim 1, McClannahan discloses that a semiconductor memory device controlled by a memory controller [fig. 5], comprising:

a delay control register [26, fig. 1] for receiving delay control information and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data [fig. 6; col. 8, lines 53-63];

wherein a delay time of the input buffer is controlled in response to an output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

McClannahan does not explicitly disclose a delay control register for receiving delay control information from the memory controller.

Ryan discloses a delay control register [131, fig. 1] for receiving delay control information from the memory controller [105, fig. 1] and storing the information; and a

delay time of the input buffer is controlled in response to an output sing of the delay control register [col. 5, lines 4-29, 55-61; col. 10, lines 4-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of McClannahan and Ryan because they are both directed to a memory device system, and the specify teachings of Ryan stated above would improve the efficiency of operation of the memory device of McClannahan by having a delay control register stored delay control information.

As per claim 2, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As per claim 3, McClannahan discloses that a memory controller for controlling memory modules [74, 74a, fig. 5], into which a plurality of semiconductor memory devices [76, fig. 5] are loaded, comprising:

a module selector [84, fig. 6] for outputting a module selection signal for selecting the memory modules in response to a clock signal [col. 9, lines 18-23];

a delay control register for receiving delay control information [col. 8, lines 42-51] and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer for delaying an internal command signal, an internal address signal, and write data in response to the output signal of the module selector and outputting the delayed write data to the semiconductor memory device [fig. 6; col. 8, lines 53-66];

wherein the delay time of the output buffer is controlled in response to the output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

McClannahan does not explicitly disclose a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules.

Ryan discloses a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules [fig. 1; col. 5, lines 4-29, 55-61; col. 10, lines 4-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of McClannahan and Ryan because they are both directed to a memory device system, and the specify teachings of Ryan stated above would improve the efficiency of operation of the memory device of McClannahan by sending delay control information from memory modules.

As per claim 4, McClannahan discloses the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the

semiconductor memory device and outputting the delayed read data to the inside of the memory controller [fig. 6; col. 8, lines 53-66].

As per claim 7, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to an output signal of the delay control register [col.6, lines 8-13; col. 8, lines 49-51]; and a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller [figures 6, 7; col. 8, lines 53-66].

As per claim 8, McClannahan discloses that a memory system [fig. 5] comprising memory modules, into which a plurality of semiconductor memory devices are loaded, and a memory controller [78, figures 5, 6] for controlling the memory modules,

wherein the memory controller comprises: a delay control register for receiving the predetermined delay information and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer, whose delay time is controlled in response to the output signal of the delay control register, the output buffer for delaying a command signal, an address signal, and write data, and outputting the delayed command signal, address signal, and write data to the semiconductor memory device [fig. 6; col. 8, lines 53-66].

McClannahan does not explicitly disclose the memory modules comprise SPDs for storing predetermined control information according to the specification of the memory module.

Ryan discloses the memory modules comprise SPDs for storing predetermined control information according to the specification of the memory module [fig. 1; col. 5, lines 4-29, 55-61; col. 10, lines 4-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of McClannahan and Ryan because they are both directed to a memory device system, and the specify teachings of Ryan stated above would improve the efficiency of operation of the memory device of McClannahan by sending delay control information from memory modules.

As per claim 9, McClannahan discloses the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the semiconductor memory device and outputting to the inside of the memory controller. [fig. 6; col. 8, lines 53-66].

As per claim 10, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to an enable signal and the output signal of the delay control register [col.6, lines 8-13; col. 8, lines 49-51]; and a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller [figures 6, 7; col. 8, lines 53-66].

As per claim 12, McClannahan discloses that each of the semiconductor memory devices comprises:

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data [fig. 6; col. 8, lines 53-63]; wherein the delay time of the input buffer is controlled in response to the output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

Ryan discloses a delay control register for receiving delay control information from the memory controller and storing the received delay control information [fig. 1; col. 5, lines 4-29, 55-61; col. 10, lines 4-9].

As per claim 13, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As to claims 14-18 and 20-22, McClannahan and Ryan basically teach the corresponding elements as set forth in claims 1-13 that are carried out the method of operating steps in claims 14-18 and 20-22. McClannahan and Ryan teach the claimed system. Therefore, McClannahan and Ryan teach the claimed method of steps to carry out the system.

7. Claims 14, 15, 24, 25, 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by McClannahan (McClannahan), U.S. patent no. 6,438,670.

As per claim 24, McClannahan discloses an integrated circuit memory system [fig. 5], comprising:

A plurality of memory modules [fig. 5, col. 8, lines 15-22], a respective one of which being responsive to a control signal and having delay information stored thereon [figures 5, 6; col. 8, lines 38-63]; and

A memory controller [78, fig. 5] that is configured to generate the control signal in response to the delay control information [col. 2, line 67-col. 3, line 7; col. 6, lines 8-13; col. 8, lines 49-51.

As per claim 25, McClannahan discloses that the memory controller further comprises: a delay control register that is configured to receive and to store the delay control information therein [fig. 1; col.6, lines 8-13; col. 8, lines 49-51]; and

an output buffer that is configured to generate the control signal in response to an input control signal and the delay control information stored in the delay control register [fig. 6; col. 8, lines 53-66].

As per claim 27, McClannahan discloses that the memory controller further comprises: an input buffer that is configured to receive data from the respective one of the plurality of memory modules at an input thereof and to provide the received data at an output thereof in response to the delay control information stored in the delay control register [fig. 6; col. 8, lines 42-66].

As per claim 28, McClannahan discloses that the control signal comprises a command control signal, an address control signal, and data, and wherein the output buffer comprises a command output buffer that is configured to generate the command

control signal in response to an input command control signal and the delay control information stored in the delay control register, an address output buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data output buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register [figures. 5-7; col. 5, lines 50-52, 61-63; col. 6, lines 19-29; col. 8, lines 53-63].

As per claim 29, McClannahan discloses that at least one of the plurality of memory modules comprises a plurality of memory devices [fig. 5; col. 8, lines 13-18].

As to claims 14, 15, 43 and 44, McClannahan basically teaches the corresponding elements as set forth in claims 24, 25 and 27-29 that are carried out the method of operating steps in claims 14, 15, 43 and 44. McClannahan teaches the claimed system. Therefore, McClannahan teaches the claimed method of steps to carry out the system.

Allowable Subject Matter

8. Claims 5, 6, 11, 19, 23, 26 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 34, 35 and 37 are allowed over prior art.

10. Applicant's arguments filed on 5/3/05, which have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

July 14, 2005